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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/718,591	11/24/2003	Tetsuhiko Azuma	245829US2	1232

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EXAMINER	
MYERS, PAUL R	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 12/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/718,591	AZUMA, TETSUHIKO	
	Examiner	Art Unit	
	Paul R. Myers	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/24/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Stiffler et al PN 4,484,273 in view of Wang 6,243,808.

In regards to claim 1: Stiffler teaches a microprocessor (100) comprising: a processor core (210) including an instruction executing unit configured to execute instructions for input and output controlling and processing for data (Column 8 lines 1-15) and a cache memory configured to store the data (250); a memory management unit (200) coupled to the processor core (210), the memory management unit configured to manage memory system including the cache memory (250); and a bus interface (265 or 270 or 265 and 270 taken together or 120) coupled to the processor core (210) and the memory management unit (200). Stiffler does not teach the bus interface configured to rearrange the bits of the data transferred to and from the processor core. Wang teaches an interface for a processor that is configured to rearrange bits of the data transferred to and from the processor (Abstract and figure 1A). It would have been obvious to include Wang's interface as the interface(s) of Stiffler because this would have allowed for fast conversion of data format to and from big endian and little endian, or any other external format.

In regards to claim 2: Stiffler teaches the interface(s) including a data input/output unit coupled to the processor core and memory management unit, configured to send and receive date. Wang teaches switching circuit (included in G1-G7) coupled to data input/output (b(0)-b(7) "word 1") the switching circuit configured to receive the data to change the order of bits of the data according to pre-routing information (C1-C3); and a bus switch (s(0)-s(7) in rows 1-3) coupled to the switching circuit, the bus switch configured to receive the data change order of bits to change the order of bits per predetermined number of bits.

In regards to claims 3, 5, 7-8, 10-13: Wang teaches routing control signals (C1-C3). Wang is silent upon the source of the routing control signals. Official Notice is taken that routing tables that control routing switches are well known. It would have been obvious to include a routing table in the MMU for the control of the switching. Stiffler also teaches the MMU translates the virtual address information into the physical addresses used for addressing main memory (Column 8 lines 16-41).

In regards to claim 4: Wang teaches the control signal changing the order of the bits.

In regards to claim 6: Wang teaches changing pre bit (Row 1).

In regards to claim 9: Wang teaches changing per bit, per nibble, pre byte, and per half word. Wand also expressly states that a progressive group size is envisioned of size N. It would have been obvious to swap per page.

3. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Stiffler et al PN 4,484,273 in view of Wang PN6,243,808 as applied to claim 1 above, and further in view of Sako et al PN 5,148,161.

In regards to claim 14: Stiffler teaches the microprocessor as described above. Wang teaches the bit swapping. Stiffler also teaches a bridge (one of 120-150), storage device/memory (165-175). Stiffler in view of Wang teaches the processor structure with bit rearrangement as claimed. Stiffler does not expressly teach the bridge having a memory for buffering the data, the processor being for video/sound, or D/A conversion. Sako teaches a video/audio processing system including a DSP with a D/A converter, bit rearrange and a buffer in an interface bridge for storing rearranged bits. It would have been obvious to include the memory management and bit rearrangement structure in the video/audio system of Sako because this would have provided for fast bit conversion and memory control.

In regards to claim 15: Stiffler teaches the interface(s) including a data input/output unit coupled to the processor core and memory management unit, configured to send and receive date. Wang teaches switching circuit (included in G1-G7) coupled to data input/output (b(0)-b(7) "word 1") the switching circuit configured to receive the data to change the order of bits of the data according to pre-routing information (C1-C3); and a bus switch (s(0)-s(7) in rows 1-3) coupled to the switching circuit, the bus switch configured to receive the data change order of bits to change the order of bits per predetermined number of bits.

In regards to claims 16, 18, 20: Wang teaches routing control signals (C1-C3). Wang is silent upon the source of the routing control signals. Official Notice is taken that routing tables that control routing switches are well known. It would have been obvious to include a routing table in the MMU for the control of the switching. Stiffler also teaches the MMU translates the virtual address information into the physical addresses used for addressing main memory (Column 8 lines 16-41).

In regards to claim 17: Wang teaches the control signal changing the order of the bits.

In regards to claim 19: Wang teaches changing pre bit (Row 1).

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul R. Myers whose telephone number is 571 272 3639. The examiner can normally be reached on Mon-Thur 6:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul R. Myers

PAUL R. MYERS
PRIMARY EXAMINER

PRM
December 5, 2005